**Timing diagram of MOV Instruction in Microprocessor**

* Difficulty Level : [Medium](https://www.geeksforgeeks.org/medium/)
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**Problem –** Draw the timing diagram of the given instruction in 8085,

MOV B, C

Given instruction copies the contents of the source register into the destination register and the contents of the source register are not altered.

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**Example:**

MOV B, C

Opcode: MOV

Operand: B and C

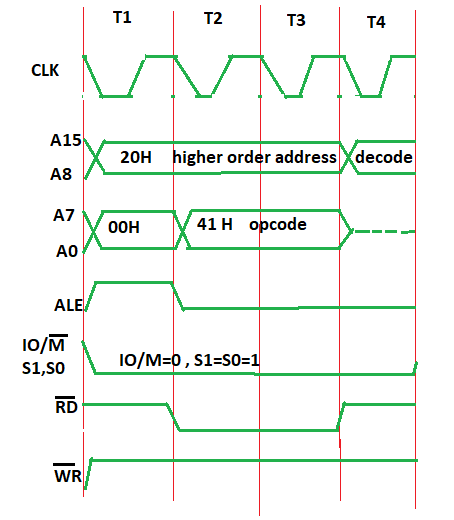
Bis the destination register and C is the source register whose contents need to be transferred to the destination register.

**Algorithm –**  
The instruction MOV B, C is of 1 byte; therefore the complete instruction will be stored in a single memory address. For example:

2000: MOV B, C

Only opcode fetching is required for this instruction and thus we need 4 T states for the timing diagram. For the opcode fetch the IO/M (low active) = 0, S1 = 1 and S0 = 1.

The timing diagram of MOV instruction is shown below:



**In Opcode fetch ( t1-t4 T states ):**

1. **00 –** lower bit of address where opcode is stored, i.e., 00
2. **20 –** higher bit of address where opcode is stored, i.e., 20.
3. **ALE –** provides signal for multiplexed address and data bus. Only in t1 it used as address bus to fetch lower bit of address otherwise it will be used as data bus.
4. **RD (low active) –** signal is 1 in t1 & t4 as no data is read by microprocessor. Signal is 0 in t2 & t3 because here the data is read by microprocessor.
5. **WR (low active) –** signal is 1 throughout, no data is written by microprocessor.
6. **IO/M (low active) –** signal is 1 in throughout because the operation is performing on memory.
7. **S0 and S1 –** both are 1 in case of opcode fetching.